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Digital I/O Unit Encoder Interface Event Capture Unit Watchdog Timer PM ROM 2k X 24 DM RAM 1k X 16 PM RAM 2k X 24 MEMORY SERIAL PORTS SPORT0 SPORT1 Precision Voltage Reference Power On Reset EXTERNAL ADDRESS BUS EXTERNAL DATA BUS Figure 4: Block Diagram For The A 2th, 2024

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Note To T-sg-9a. V7, V8, Loop Numbering-8 Phase Phase Diagram And Typical Rev. 7-12-17: Moved Nema 8 P3 For Button Push Spare (orange) Neutral (white) P4 * 9c Or 12c May Be Used For Button Push Button Push Single Aps Pushbutton Double Ap 2th, 2024

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