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STM32MP1-Memory-DDR Controller And PHY DDR ...

The DDR Subsystem (DDRSS) Is Composed Of 2 Main Parts: • The DDR Controller (DDCTRL) • The DDR PHY (DDRPHYC) DFI Is The Standard Interface Between The DDR Controller And The DDR PHY The DDRCTRL Is In Charge Of: • Convert AXI Bus Transactions To DRAM Transfers At DFI Interface • AXI Jan 12th, 2024

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Rich Set Of Capabilities For Configuring, Testing, And Optimizing Your DDR Memory And PHY. Figure 1: PFx System Overview. DDR Tuning And Calibration Guide On Zynq -7000 . 8 The Output Format Will Vary Based Upon The Architecture. DD Apr 11th, 2024

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