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Electronics And Communication Engineering Department 2nd Year 2nd Semester: A. Theory Sl. No. Course Code Course Name Contact Hours/Week Credit L T P Total Points

Sl. No.	Course Code	Course Name	Contact Hours/Week	Credit	L	T	P	Total Points
1	CHEM2001	Basic Environmental Engineering And Ecology	3 0 0	3	3	2		
	ECEN2201	EM Theory & Transmission Line	3 0 0	3	3	3		
	ECEN2202	Digital Electronics	3 0 0	3	3	3		
	ECEN2203	Analog Communication	3 0 0	3	3	5		
	ECEN2204	Solid State Devices	3 0 0	3	3	3		

May 3th, 2024 Department Of Electronics And Communication Engineering

4. G.F.Sudha And B.Nanchariah, "A Distributed Routing Algorithm For Data Gram Traffic In Teledesic System", International Conference On Wireless Communication Networks, SSN College Of Engineering, Chennai, 27-28 June 2003.

5. G.F.Sudha And T.G.Palanivelu, "Visibility Enhancement Of Subsurface Tissue Images", Feb 4th, 2024 DEPARTMENT OF ELECTRONICS AND COMMUNICATION ... Using Lab View 8.6, International Journal Of Electronics, Communication & Instrumentation Engineering Research And Development (IJEIERD) Jun 2013, Vol. 3, Issue 2, Pp:195-200.

3. K.SudhaRani, T. C. Sarma & K.Satya Prasad, Text File Encryption Using FFT Technique In Lab View 8.6, Intern May 2th, 2024.

Department Of Electronics And Communication M.Tech In ... 1 Introduction To Embedded Systems Shibu K V Tata McGraw Hill Education Private Limited, 2009 . SRI SIDDHARTHA INSTITUTE OF TECHNOLOGY- TUMAKURU (A Constituent College Of Siddhartha Aca Apr 4th, 2024 Department Of Electronics And Communication Engineering ... EMBEDDED SYSTEMS LAB MANUAL (On ARM Microcontroller And RTOS) I Year M.Tech I - Sem Prepared By Ch. Madhuri Devi Asso.Prof Easari. Parushuramu Asst.Proff Under Prof. K. Ashok Babu HOD Of ECE Dept. Sriindu College Of Engineering And Technology (an Autonomous Institution Under JNTUH) S Mar 4th, 2024 DEPARTMENT OF ELECTRONICS AND COMMUNICATION Full Adder Using (i) Basic Logic Gates And (ii) NAND Gates. (b) Full Subtractor Using (i) Basic Logic Gates And (ii) NANAD Gates. 3 Design And Implement 4-bit Parallel Adder/ Subtractor Using IC 7483. 4 Design And Implementation Of 5-bit Magnitude Comparator Using IC 7485. Realize 5 (a) Adder ... Apr 1th, 2024.

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Engineering LAB ...2. Digital Storage Oscilloscope (DSO) 3. Power Supply 4. Patch Cords Procedure: 1. The Connections Are Given As Per The Block Diagram For Natural Sampling 2. Connect The Power Supply In Proper Polarity To The Kit And Switch It On. 3. Using The Clock Selector Switch Select 8 KHz Sampling Frequency And Using Switch SW2 Select 50% Duty Cycle. Feb 7th, 2024.

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