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Chapter 8 Memory Hierarchy And Cache Memory

• Suppose Processor Has 2 Levels Of Hierarchy: Cache And Main Memory • T Cache = 1 Cycle, T MM = 100 Cycles • What Is The AMAT Of The Program From Example 1? AMAT = T Cache + MR Cache (t MM) = [1 + 0.375(100)] Cycles = 38.5 Cycles Memory Performance Example 2 May 3th, 2024

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Only 1 Layer (contact Mask) Is Used To Program Memory Array Programming Of The Memory Can Be Delayed To One Of Last Process Steps ROM Layout Precharged ROM WL[0] WL[1] WL[2] WL[3] BL[0] BL[1] BL[2] BL[3] GND GND VDD Precharge Devices opre PMOS Precharge Device Can Be Made As Large Jan 8th, 2024

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Memory H10 With Solid State Storage Prevails For The Majority (more Than 50%) Of The Iometertests (including Both Single And Mixed Modes) Combined, For The Majority Of The Collection Of Benchmarks And Real-world Workloads Co Mar 7th, 2024

The Memory/Storage Hierarchy And Virtual Memory

Storage Device Speed Vs. Size Facts: •CPU Needs Sub-nanosecond Access To Data To Run Instructions At Full Speed •Faststorage (sub-nanosecond) Is Small (100-1000 Bytes) •Big Storage (gigabytes) Is Slow (15 Nanoseconds) •Hugestorage (terabytes) Is Glaciallyslow (milliseconds) Goal: •Need Many Gigabytes Of Memory Feb 16th, 2024

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Secondary Memory Memory Hierarchy

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Cache Memory And Performance Memory Hierarchy 1

Memory Hierarchy 19 CS@VT Computer Organization II © 2005-2015 CS:APP & McQuain Caches Cache: A Smaller, Faster Storage Device That Acts As A Staging Area For A Subset Of The Data In A Larger, Slower Device. Fundamental Idea Of A Memory Hierarchy: – For Each K, The Faster, Smaller Device At Level K Serv Apr 5th, 2024

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